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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,239	04/23/2004	Huilong Zhu	FIS920030375	3238

23389 7590 02/07/2006

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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,239	ZHU ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *14-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/15/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group II, claims 1-13 in the reply filed on November 21, 2006 is acknowledged.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The Rejections

Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Dresselhaus et al. (U.S. 6,060,656).

Dresselhaus a superlattice structure with

(1) a substrate of either bulk silicon (Si) or silicon on insulator (SOI), and a gate dielectric layer over the substrate;

a stacked gate structure of SiGe and/or Si:C to produce stresses by the structures of Ssi(strained Si)/SiGe or SSi/Si:C in the stacked gate structure and having a first stressed film layer of large grain size Si or SiGe over the gate dielectric layer,

a second stressed film layer of strained SiGe or strained Si:C over the first stressed film layer, and

a semiconductor or conductor such as p(poly)-Si over the second stressed film layer (see column 6, lines 28-46. Figure 4);

(2) wherein stress is produced in the stacked gate structure by different semiconductor materials and/or by different percentages of semiconductor materials (see column 6, lines 28-46);

(3) the device fabricated on a chip having both nFET devices and PFET devices, and wherein the NFET devices and PFET devices have different stresses (see column 6, lines 28-46. Figure 4);

(4) wherein the stacked gate structure of the nFET devices comprises the second stressed film layer of strained SiGe over the first stressed film layer of single crystal silicon, and the stacked gate structure of the PFET devices comprises the second stressed film layer of strained Si:C over the first stressed film layer of single crystal silicon (see column 6, lines 28-46. Figure 4);

(5) wherein the stacked gate structure of the nFET devices comprises the second stressed film layer of strained $Si_{1-y}Ge_y$ over the first stressed film layer of strained $Si_{1-x}Ge_x$, and the stacked gate structure of the PFET devices comprises the second stressed film layer of strained $Si_{1-z}Ge_z$ over the first stressed film layer of strained $Si_{1-x}Ge_x$, wherein $y>x$ and $z<x$ to produce different stresses (see column 6, lines 28-46. Figure 4);

(6) wherein the value of x is selected to adjust the PFET Vt (threshold voltage) (see column 6, lines 28-46. Figure 4);

(7) wherein the Si_{1-x} Ge_x is a seed layer for parts of the gate above the Si_{1-x} Ge_x layer, and the Si_{1-x} Ge_x layer is strained after selective epitaxial growth (see column 6, lines 28-46. Figure 4);

(8) wherein the stacked gate structure of the nFET devices comprises the second stressed film layer of strained $Si_{1-y}Ge_y$ over the first stressed film layer of strained $Si_{1-xn}Ge_{xn}$, and the stacked gate structure of the PFET devices comprises the second stressed film layer of strained $Si_{1-z}Ge_z$ over the first stressed film layer of strained $Si_{1-xp}Ge_{xp}$, wherein y>xn and z<xp, to produce stresses (see column 6, lines 28-46. Figure 4);

(9) wherein the $Si_{1-xn}Ge_{xn}$ is a seed layer for parts of the gate above the $Si_{1-xn}Ge_{xn}$ seed layer and the $Si_{1-xn}Ge_{xn}$ seed layer seed layer is strained after selective epitaxial growth, and the $Si_{1-xp}Ge_{xp}$ is a seed layer for parts of the gate above the $Si_{1-xp}Ge_{xp}$ seed layer and the $Si_{1-xp}Ge_{xp}$ seed layer is strained after selective epitaxial growth (see column 6, lines 28-46. Figure 4);

(10) wherein the stacked gate structure of the nFET devices comprises the second stressed film layer of strained $Si_{1-y}Ge_y$ over the first stressed film layer of strained Si_{1-x} Ge_x, and the stacked gate structure of the PFET devices comprises the second stressed film layer of strained Si:C over the first stressed film layer of strained Si_{1-x} Ge_x , wherein y>x and z<x, to produce different stresses (see column 6, lines 28-46. Figure 4);

(11) the device fabricated in an integrated circuit PFET devices having comprising both nFET devices and said stacked gate structure (see column 6, lines 28-46. Figure 4);

(12) the device fabricated in an integrated circuit comprising nFET devices having said stacked gate structure (see column 6, lines 28-46. Figure 4);

(13) the device fabricated in an integrated circuit comprising PFET devices having said stacked gate structure (see column 6, lines 28-46. Figure 4).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
February 3, 2006